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To: Commissioner for Patents for **Examiner Trisha U. Vu** **Group Art Unit 2112**	Facsimile No.: **703/872-9306**
From: Michele Morrow Legal Assistant to Francis Lammes	No. of Pages Including Cover Sheet: **26**

Message:

Enclosed herewith:

- Transmittal Document; and
- Appeal Brief.

Re: Application No. **09/881,922**
Attorney Docket No: **AUS920010332US1**

Date: Thursday, January 06, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Capps, Jr. et al.**	§	Group Art Unit: **2112**
Serial No.: **09/881,922**	§	Examiner: **Vu, Trisha U.**
Filed: **June 14, 2001**	§	Attorney Docket No.: **AUS920010332US1**
For: **Method and System for System Performance Optimization Via Heuristically Optimized Buses**	§	

35525
PATENT TRADEMARK OFFICE
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By: Michele Morrow
Michele Morrow

TRANSMITTAL DOCUMENT

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- Appeal Brief (37 C.F.R. 41.37).

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Respectfully submitted,

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Docket No. AUS920010332US1 *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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By: Michele Morrow
Michele Morrow

APPEAL BRIEF (37 C.F.R. 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on November 12, 2004.

The fees required under § 41.20(B)(2), and any required petition for extension of time for filing this brief and fees therefore, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

REAL PARTY IN INTEREST

The real party in interest in this appeal is the following party: International Business Machines Corporation.

RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such appeals or interferences.

STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-22

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims canceled: NONE
2. Claims withdrawn from consideration but not canceled: NONE
3. Claims pending: 1-22
4. Claims allowed: NONE
5. Claims rejected: 1-22

C. CLAIMS ON APPEAL

The claims on appeal are: 1-22

STATUS OF AMENDMENTS

There are no amendments after the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1:

The present invention provides for enhancing performance of a bus in a data processing system. (Specification, page 4, lines 3-4) The present invention monitors data flow through an adapter coupled to the bus in a data processing system. (Specification, page 12, line 24 to page 13, line 3) The present invention determines if increased bus performance is desirable. (Specification, page 15, lines 3-17) If an increase in bus performance is desired, the present invention hands off control to a code module which enhances the performance of the bus. (Specification, page 15, lines 6-12) The code module for heuristic bus optimization includes a performance optimizer unit, a hardware bus control unit coupled to the performance optimizer unit, and a process management unit managing at least one device driver. (Specification, page 13, line 16 to page 14, line 13)

Independent claim 9:

The present invention provides a system for optimizing the performance of a bus. (Specification, page 4, lines 3-4) The present invention has a first bus coupled to at least one central processing unit (CPU) having a code module embedded therein. (Specification, page 11, line 26 to page 12, line 5) The present invention has at least one input/output (I/O) adapter coupled to the first bus. (Specification, page 12, line 24 to page 13, line 3) The present invention has a driver for the at least one input/output (I/O) adapter residing in the at least one central processing unit (CPU). (Specification, page 11, line 26 to page 12, line 23) The present invention has a bus monitor coupled to a hardware bus control unit residing in the code module wherein information acquired by the bus monitor is processed, and a decision is made to increase adapter throughput. (Specification, page 12, line 20 to page 13, line 3)

Independent claim 15:

The present invention provides a code module for heuristic bus optimization. (Specification, page 11, line 26 to page 12, line 3) The present invention provides a performance optimizer unit, a hardware bus control unit coupled to the performance optimizer unit and a process management unit managing at least one device driver. (Specification, page 11, line 26 to page 13, line 3)

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection on appeal are as follows:

- Claims 1-4, 8-10, 15 and 18-21 are rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Brown et al. (U.S. Patent No. 6,075,772);
- Claims 5, 11-13, 16 and 17 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Jeddeloh (U.S. Patent No. 6,363,445);
- Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Harper et al. (U.S. Patent No. 5,481,755);
- Claims 14 and 22 are rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Burns et al. (U.S. Patent No. 6,134,624).

ARGUMENT

The Final Office Action rejects claims 1-4, 8-10, 15 and 18-21 under 35 U.S.C. § 102(b) as being allegedly anticipated by Brown et al. (U.S. Patent No. 6,075,772); rejects claims 5, 11-13 and 16-17 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Jeddeloh (U.S. Patent No. 6,363,445 B1); rejects claims 6 and 7 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Harper et al. (U.S. Patent No. 5,481,755); and rejects claims 14 and 22 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Burns et al. (U.S. Patent No. 6,134,624).

Brown is directed to a method that controls the data rate through a communications adapter having a guaranteed bandwidth connection. The data rate is controlled by assigning to the guaranteed bandwidth connection, a maximum threshold value proportional to the amount of data to be transmitted through the communications adapter in a time interval to satisfy the guaranteed bandwidth of the connection. The amount of data transmitted through the communications adapter for the guaranteed bandwidth connection is then counted so as to provide a connection data count associated with the guaranteed bandwidth.

I. 35 U.S.C. § 102, Alleged Anticipation, Claims 1-4, 8-10, 15 and 18-21

Claim 1 reads as follows:

> 1. A method for enhancing performance of a bus in a data processing system, comprising:
> monitoring data flow through an adapter coupled to the bus in a data processing system;
> determining if increased bus performance is desirable; and
> handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable.

Appellants respectfully submit that Brown does not identically show each and every claim feature as they are arranged in the claims. Specifically, Brown does not teach monitoring data flow through an adapter coupled to the bus in a data processing system, determining if increased

bus performance is desirable, and handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable.

The Final Office Action alleges that Brown teaches an adapter coupled to a bus through which data flow is monitored at column 6, lines 5-10, which reads as follows:

> FIG. 1 also illustrates maximum data counters 22a and 22b. The counters 22a and 22b are associated with guaranteed bandwidth connections using the DLC layer 20 and count the amount of data in a given interval of time which is transmitted to the adapter 30 for a guaranteed bandwidth connection.

In this section, Brown is describing that an adapter is connected to the DLC layer of the computer. The Dynamic Link Control layer is not a bus. The DLC layer is defined as the layer where data packets are encoded and decoded into bits. The DLC layer furnishes transmission protocol knowledge and management and handles errors in the physical layer, flow control and frame synchronization. In contradistinction, a bus is a hardware device defined as one of the sets of conductors connecting the various functional units in a computer. Thus, Brown does not teach an adapter coupled to a bus through which data flow is monitored. Moreover, nowhere in the Brown reference is a bus even mentioned.

In response to these arguments, the Examiner states:

> ... it is noted that the Examiner addresses very clearly in the Interview that there must be a bus coupling the adapter (30 to the Data Processing System (note at least col. 2, lines 59-65 and col. 6, lines 48-60, wherein data transmitted for the adapter associated with the connection between the adapter and the associated Application 12, 14 and 16 is monitored).

In the April 20, 2004 interview, Appellants respectfully submitted to the Examiner that a prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. Nowhere in the Brown reference is an adapter coupled to a bus taught. In fact, the term "bus" does not appear in any section of the Brown reference. The sections of Brown that are cited as teaching an adapter coupled to a bus through which data flow is monitored read as follows:

> Data transmitted for the communications adapter associated with the guaranteed bandwidth connection is not transmitted to the adapter if transmission of the data would cause the connection data count to exceed the maximum

> threshold value assigned to the guaranteed bandwidth connection. The connection data count is then reset after expiration of the time interval.

(Column 2, lines 59-65)

> For example, application 12 of FIG. 1 may require a guaranteed bandwidth connection of 1.5 MB/sec. Buffers 42a would be assigned by adapter 30 to the guaranteed bandwidth connection associated with application 12. Similarly, counter 22a in the DLC layer 20 may be associated with the guaranteed bandwidth connection. Application 14 may also require a guaranteed bandwidth connection which may be 2 Mb/sec. Buffers 42b and counter 22b would be allocated to the guaranteed bandwidth connection associated with application 14. Finally, application 16 may require a best efforts connection through adapter 30. The adapter 30 would then assign the best efforts buffers 40 to the connection associated with application 16. No counter is required for best effort communications.

(Column 6, lines 48-60)

In these sections, Brown describes an adapter that is "connected" to the DLC layer of the computer. The Dynamic Link Control layer is not a bus. Furthermore, the adapter is monitoring the communications bandwidth used by various applications through the adapter and not the data flow of a bus, which is acknowledged in the Examiner's response.

Furthermore, Brown does not teach determining if increased bus performance is desirable. The Final Office Action alleges that this feature is taught at column 9, lines 11-18, which reads as follows:

> FIG. 4 illustrates the operations of an adapter 30 according to the present invention. As seen in FIG. 4, when a request for a connection is received by adapter 30, the adapter checks to see if the request of for a guaranteed bandwidth connection (block 50). If the request is not for a guaranteed bandwidth connection, then the request is processed as a standard best efforts connection and the connection is established (block 60).

In this section, Brown is merely describing that the adapter, which is "connected" to the DLC layer, is monitoring a connection request to see if the request is for a guaranteed bandwidth connection. In addition to the adapter not being coupled to a bus, the adapter is not monitoring data flow of the bus, nor is it determining if increased bus performance is desirable. The adapter of Brown is merely determining if a communications connection should be of guaranteed bandwidth or not.

In response to these arguments, the Examiner states:

> ...see the argument above, and also note at least col. 7, lines 3-37 "the adapter is then used to determine a timer value T which establishes a predefined time interval and a maximum data count for each guaranteed bandwidth connection").

Appellants respectfully submit that the section of Brown quoted by the Examiner provides clear evidence that Brown is only concerned with providing proper communications bandwidth for the communication of resident applications and is not considered with bus performance. Communications is only a part of the various activities that are running on a computer. The present invention is concerned with determining if increased bus performance is desirable.

Still further, Brown does not teach handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable. The Final Office Action alleges that this feature is taught at column 7, lines 7-37, which reads as follows:

> Operation of one embodiment of the present invention will now be described with respect to FIG. 3, which illustrated the operations of the DLC layer 20 of FIG. 1. As seen in FIG. 3, the DLC layer 20 obtains adapter information (block 58 of FIG. 4) for the adapter 30 (block 70). In the OSA adapter example, when a data processing system is established as a user of OSA a signal called Activate SAP is sent to the adapter. On the reply to this request OSA provides the OSA transmit capacity and the total OSA capacity. This information may then be utilized as discussed below to establish the appropriate thresholds.
>
> The adapter information, along with information on the time to transmit data to the adapter is then used to determine a timer value T which establishes a predefined time interval and a maximum data count for each guaranteed bandwidth connection N_i where i is the i^{th} guaranteed bandwidth connection (block 72). The maximum data count N_i acts as a maximum threshold value. N_i and T values are preferably selected based upon the amount of buffers allocated to the connection, the time to transmit data to the adapter and the service time for the data once it has reached the adapter. The interval T and the maximum data count N_i are preferably selected so that the average queue length in the adapter (the amount of buffers used for the connection) does not exceed a specified percentage of the available buffers. Preferably, the same T values is utilized for each guaranteed bandwidth connection of an adapter. Furthermore, the value of T may be predefined in both the adapter 30 and the DLC layer 20. However, in such a case the flexibility to handle various adapters with differing amounts of memory may be reduced.

In this section, Brown is merely describing the process for the guaranteed bandwidth connection through the DLC layer. As shown above, the DLC layer is not a bus and monitoring a

communication connection is not equivalent to monitoring the data flow of the bus. Additionally, nowhere in this section, or any other section of Brown, is enhancing the performance of the bus taught. Brown also fails to teach handing off control to a code module that enhances the performance of the bus if increased bus performance is desirable.

Independent claims 9 and 15 recite similar features in their respective claim terminology. Claim 9 recites "at least one input/output (I/O) adapter coupled to the first bus." Claim 15 recites "a performance optimizer unit and a hardware bus control unit coupled to the performance optimizer unit." As shown above, the adapter of Brown is connected through the DLC layer and not the physical layer where the bus resides.

Thus, Brown does not teach each and every feature of independent claims 1, 9 and 15 as is required under 35 U.S.C. § 102. At least by virtue of their dependency on independent claims 1, 9 and 15, respectively, Brown does not teach each and every feature of dependent claims 2-4, 8, 10 and 18-21. Accordingly, Appellants respectfully request withdrawal of the rejection of claims 1-4, 8-10, 15 and 18-21 under 35 U.S.C. § 102.

Furthermore, Brown does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Absent the Examiner pointing out some teaching or incentive to implement Brown such that, an adapter is coupled to the bus in a data processing system through which data flow is monitored, determining if increased bus performance is desirable, and handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable, one of ordinary skill in the art would not be led to modify Brown to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion, or incentive to modify Brown in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the Appellants' disclosure as a template to make the necessary changes to reach the claimed invention.

I.A. 35 U.S.C. § 102, Alleged Anticipation of Claim 3

With regard to claim 3, Brown does not teach changing, in small incremental steps, hardware settings upstream to the adapter; and after an optimum performance point is achieved,

maintaining current state. The Final Office Action alleges that these features are taught at column 8, lines 3-6, and column 8, line 48 to column 9, line 3, which read as follows:

> If the guaranteed bandwidth connection was incorrectly utilized for the previous interval, then the DLC layer 20 may compensate for the incorrect utilization of the connection by modifying the value of Ni for the next interval (block 88).

Column 8, lines 3-6.

> As will be appreciated by those of skill in the art, the present invention provides for packets of data to be transmitted to the communications adapter 30 by the DLC layer 20. These packets of data are typically in a predefined size for a given connection. The fixed size nature of the data packets results in the possibility that the maximum data count may not fall on a packet boundary. For example, to a guaranteed bandwidth connection is a 1.5 Mb/sec. connection and the interval is 0.1 seconds, then the present invention would 150 Kb per interval to be transmitted for the connection. However, if the packet size is 4 Kb then the count will reach 148 Kb and the next packet will cause the maximum count to be exceeded. Preferably, the additional packet will not be sent to the adapter and the count will not be exceeded. However, if the additional packet is accepted and the count exceeded, on the next interval, the starting count for the connection will be adjusted to reflect the over-utilization of the connection on the previous interval and the start count could be set to 2 Kb to compensate for the additional data of the previous interval. Alternatively, the maximum threshold could be set to 148 Kb to compensate for the additional 2 Kb transmitted during the previous interval.

Column 8, lines 48 to column 9, line 3. In these sections, Brown is merely describing changes made in the DLC layer. As shown above, the DLC layer is a software layer and any changes made in this layer are changes to software settings. In contradistinction, the claims recite changiong, in small incremental steps, hardware settings upstream to the adapter; and after an optimum performance point is achieved, maintaining a current state.

I.B. 35 U.S.C. § 102, Alleged Anticipation of Claim 4

With regard to claim 4, Brown does not teach determining whether the performance is a function of an external device connected to the adapter. The Final Office Action alleges that this feature is taught at column 8, lines 46-67, shown above. In this section, Brown is monitoring the throughput of an adapter; there is nothing in this section, or any other section of Brown, that

teaches determining whether the performance is a function of an external device connected to the adapter.

I.C. 35 U.S.C. § 102, Alleged Anticipation of Claims 10 and 18-21

As a further example, with regard to claims 10 and 18-21, Brown does not teach a bus connected to an adapter or is a bus even mentioned, as shown above. Thus, Brown does not teach a second bus disposed to be monitored by the bus monitor, and connected to the at least one input/output (I/O) adapter, as recited in claim 10. Nor does Brown teach "determining whether bus performance is maximized", as recited in claim 18; "passing at least one parameter to the hardware bus control unit", as recited in claim 19; "a hardware bus control unit reading bus performance", as recited in claim 20; and, "changing at least one bus parameter in an I/O adapter", as recited in claim 21.

II. 35 U.S.C. § 103, Alleged Obviousness, Claims 5, 11-13 and 16-17

The Final Office Action rejects claims 5, 11-13 and 16-17 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Jeddeloh (U.S. Patent No. 6,363,445 B1). This rejection is respectfully traversed.

Claims 5, 11-13 and 16-17 are dependent on independent claims 1, 9 and 15 and, thus, these claims distinguish over Brown for at least the reasons noted above with regards to claims 1, 9 and 15. Moreover, Jeddeloh does not provide for the deficiencies of Brown and, thus, any alleged combination of Brown and Jeddeloh would not be sufficient to reject independent claims 1, 9 and 15 or claims 5, 11-13 and 16-17 by virtue of their dependency. That is, Jeddeloh does not teach monitoring data flow through an adapter coupled to the bus in a data processing system, determining if increased bus performance is desirable, and handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable.

Moreover, the Final Office Action may not use the claimed invention as an "instruction manual" or "template" to piece together the teachings of the prior art so that the invention is rendered obvious. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Such

reliance is an impermissible use of hindsight with the benefit of Applicant's disclosure. *Id.* Therefore, absent some teaching, suggestion, or incentive in the prior art, Brown and Jeddeloh cannot be properly combined to form the claimed invention. As a result, absent any teaching, suggestion, or incentive from the prior art to make the proposed combination, the presently claimed invention can be reached only through an impermissible use of hindsight with the benefit of Applicant's disclosure a model for the needed changes.

In view of the above, Brown and Jeddeloh, taken either alone or in combination, fail to teach or suggest the specific features recited in independent claims 1, 9 and 15, from which claims 5, 11-13 and 16-17 depend. Accordingly, Appellants respectfully request withdrawal of the rejection of claims 5, 11-13 and 16-17 under 35 U.S.C. § 103.

III. 35 U.S.C. § 103, Alleged Obviousness, Claims 6 and 7

The Final Office Action rejects claims 6 and 7 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Harper et al. (U.S. Patent No. 5,481,755). This rejection is respectfully traversed.

Claims 6 and 7 are dependent on independent claim 1 and, thus, these claims distinguish over Brown for at least the reasons noted above with regards to claim 1. Moreover, Harper does not provide for the deficiencies of Brown and, thus, any alleged combination of Brown and Harper would not be sufficient to reject independent claim 1 or claims 6 and 7 by virtue of their dependency. That is, Harper does not teach monitoring data flow through an adapter coupled to the bus in a data processing system, determining if increased bus performance is desirable, and handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable.

Moreover, the Final Office Action may not use the claimed invention as an "instruction manual" or "template" to piece together the teachings of the prior art so that the invention is rendered obvious. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Such reliance is an impermissible use of hindsight with the benefit of Applicant's disclosure. *Id.* Therefore, absent some teaching, suggestion, or incentive in the prior art, Brown and Harper cannot be properly combined to form the claimed invention. As a result, absent any teaching,

suggestion, or incentive from the prior art to make the proposed combination, the presently claimed invention can be reached only through an impermissible use of hindsight with the benefit of Applicant's disclosure a model for the needed changes.

In view of the above, Brown and Harper, taken either alone or in combination, fail to teach or suggest the specific features recited in independent claim 1, from which claims 6 and 7 depend. Accordingly, Appellants respectfully request withdrawal of the rejection of claims 6 and 7 under 35 U.S.C. § 103.

IV. 35 U.S.C. § 103, Alleged Obviousness, Claims 14 and 22

The Final Office Action rejects claims 14 and 22 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Brown et al. (U.S. Patent No. 6,075,772) and further in view of Burns et al. (U.S. Patent No. 6,134,624). This rejection is respectfully traversed.

Claims 14 and 22 are dependent on independent claims 9 and 15 and, thus, these claims distinguish over Brown for at least the reasons noted above with regards to claims 9 and 15. Moreover, Burns does not provide for the deficiencies of Brown and, thus, any alleged combination of Brown and Burns would not be sufficient to reject independent claims 9 and 15 or claims 14 and 22 by virtue of their dependency. That is, Burns does not teach "at least one input/output (I/O) adapter coupled to the first bus", as recited in claim 9 and "a performance optimizer unit and a hardware bus control unit coupled to the performance optimizer unit", as recited in claim 15.

Moreover, the Final Office Action may not use the claimed invention as an "instruction manual" or "template" to piece together the teachings of the prior art so that the invention is rendered obvious. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). Such reliance is an impermissible use of hindsight with the benefit of Applicant's disclosure. *Id.* Therefore, absent some teaching, suggestion, or incentive in the prior art, Brown and Burns cannot be properly combined to form the claimed invention. As a result, absent any teaching, suggestion, or incentive from the prior art to make the proposed combination, the presently claimed invention can be reached only through an impermissible use of hindsight with the benefit of Applicant's disclosure a model for the needed changes.

In view of the above, Brown and Burns, taken either alone or in combination, fail to teach or suggest the specific features recited in independent claims 9 and 15, from which claims 14 and 22 depend. Accordingly, Appellants respectfully request withdrawal of the rejection of claims 14 and 22 under 35 U.S.C. § 103.

CONCLUSION

In view of the above, Appellants respectfully submit that claims 1-22 are allowable over the cited prior art and that the application is in condition for allowance. Accordingly, Appellants respectfully request the Board of Patent Appeals and Interferences to not sustain the rejections set forth in the Final Office Action.

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CLAIMS APPENDIX

The text of the claims involved in the appeal are:

1. A method for enhancing performance of a bus in a data processing system, comprising:

monitoring data flow through an adapter coupled to the bus in a data processing system;

determining if increased bus performance is desirable; and

handing off control to a code module which enhances the performance of the bus if increased bus performance is desirable.

2. The method of claim 1, further comprising:

determining the performance by examining prior throughput of data of the adapter.

3. The method of claim 1, further comprising:

changing, in small incremental steps, hardware settings upstream to the adapter; and

after an optimum performance point is achieved, maintaining current state.

4. The method of claim 1, further comprising:

determining whether the performance is a function of an external device connected to the adapter.

5. The method of claim 1, further comprising:

reaching a decision based upon prior performance parameters of other devices coupled to the bus.

6. The method of claim 1, further comprising:

determining a priority of a set of adapters, including the adapter, coupled to the bus.

7. The method of claim 6, further comprising:

changing the priority throughput of at least one of the set of adapters.

8. The method of claim 1, further comprising:

simultaneously monitoring throughput of the adapter.

9. A system for optimizing the performance of a bus, comprising:

a first bus coupled to at least one central processing unit(CPU)having a code module embedded therein;

at least one input/output (I/O) adapter coupled to the first bus;

a driver for the at least one input/output (I/O) adapter residing in the at least one central processing unit (CPU); and

a bus monitor coupled to a hardware bus control unit residing in the code module wherein information acquired by the bus monitor is processed, and a decision is made to increase adapter throughput.

10. The system of claim 9, further comprising a second bus disposed to be monitored by the bus monitor, and connected to the at least one input/output (I/O) adapter.

11. The system of claim 9, wherein the code module comprises:

a performance optimizer unit, wherein a process management queue is scanned, a determination as to weather the process management queue have a high priority I/O process;

a process management unit coupled to the performance optimizer unit; and

a hardware bus control unit, wherein bus performance is being read, coupled to the performance optimizer unit.

12. The system of claim 11, further comprising device driver, wherein at least one bus parameter in the I/O adapter is changed, coupled to the process management unit.

13. The system of claim 11, wherein the hardware bus control unit changes at least one bus parameter.

14. The system of claim 9, wherein the hardware bus control unit is coupled to an I/O bus hub.

15. A code module for heuristic bus optimization, comprising:

a performance optimizer unit;

a hardware bus control unit coupled to the performance optimizer unit; and

a process management unit managing at least one device driver.

16. The code module of claim 15, wherein the performance optimizer unit scans a process management queue and determines whether the process management queue includes a high priority I/O process.

17. The code module of claim 15, wherein the performance optimizer unit queries the hardware bus control unit for bus performance of I/O devices.

18. The code module of claim 15, wherein the performance optimizer unit determines whether bus performance is maximized for the most critical I/O process.

19. The code module of claim 15, wherein the performance optimizer unit passes at least one parameter to the hardware bus control unit and the at least one device driver.

20. The code module of claim 15, wherein the hardware bus control unit reads bus performance.

21. The code module of claim 15, wherein the at least one device driver changes at least one bus parameter in an I/O adapter.

22. The code module of claim 15, wherein the hardware bus control unit changes at least one bus parameter in an I/O bus hub.

EVIDENCE APPENDIX

There is no evidence to be presented.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.